# *High-Speed Digital in PathWave ADS class*

## Why is high-speed digital design important?

When digital signals reach gigabit speeds, unpredictability becomes the norm. Potential Signal Integrity issues require evaluation throughout all stages of your project. The process of getting your design back on track starts with the best tools for the job.

Keysight's high-speed digital solution set is a range of essential tools, for both measurement and simulation that will help you cut through the challenges of gigabit digital designs. Our tools provide views into time and frequency domains revealing underlying problems and ensuring compliant designs. With Keysight, you'll be equipped to pinpoint problems, optimize the design, and deliver on time.

## What you will learn

This course starts with ADS basics, covering workspaces, libraries, cells and technologies. It covers the usage of layout in ADS, to perform some basics operations (editing, booleans,..).

The second day will be focused on the pre-layout phase in SI/HSD engineer job and to show the flow use in ADS to succeed in this step through in depth presentations and labs.

Channel simulator with IBIS-AMI will be used and explained.

The third day of the course covers SIPro and PiPro analysis capabilities, Power Aware SI analysis capability tuned to the HSD application to characterize the behavior of real world PCB designs imported into ADS.

## Course Type

User/Application Training

## Course Format

The course combines Lecture presentations with instructor guided hands-on sessions. **Participants will have the opportunity to perform hands-on exercises in the ADS software.**

## Audience

Designers interested in understanding how to design pre-layout with ADS, to use Channel Simulation, IBIS-AMI models, to import board from other PCB tools and to analyze in ADS in post-layout phase with electromagnetic models (EM model).

This training class is designed primarily for SI/PI/HSD engineers. Experience with the Advanced Design System but not required.

## Prerequisites

Good understanding of time-domain simulation

## Course Length

3 days

For registration or information please contact your training center
At : pdl-pathwave-design-software-training@keysight.com

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| | Detailed Agenda |
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| ☐ **Day 1**<br><br>**9AM – 5PM** | **Introduction to ADS environment**<br>– create an L-C ladder segment, parameterize it, convert it to a transmission line model by copy step/repeat.<br>– Use the analytical results for TL's, compute Z0/beta and demonstrate behavior of this ideal line vs. frequency and then in time-domain using a transient analysis with a bit sequence.<br>– learn how to create schematics, data display for freq/time domains, tuning, parameterization.<br>– introduce distributed components as multilayer/microstrip/striplines, and concept of impedance mismatch<br><br>**Basics of layout**<br><br>WYSIWYG vs. net-based mode, technology files, ODB++ import, navigator, how to define net names (Lab with Panda Board) |
| ☐ **Day 2**<br><br>**One day Pre-Layout**<br><br>**9AM – 5PM** | **The Channel**<br>– Designing Pre-layout for PCB Constraints<br>Interconnect Utility Tools to Build the Channel:<br>– Line characterization<br>– Using and understanding the ADS multilayer library.<br>– Via Designer<br>– The SnP component and S-parameter Checker<br>Lab: All in one pre-layout flow, sharing a common substrate stack up definition, taking previously created CILD and Via models and simulate for eye density. Optimize for system-metrics like eye height and width, with parameterized transmission lines, via designs and Tx/Rx EQ using Signal integrity application build in Design guides<br>- HSD Simulation<br>Use the Pre-layout Schematic to build the channel<br>– Transient Simulation using IBIS Models<br>– Channel Simulation including Ibis AMI Model (Lecture about IBIS-AMI and why you need it).<br>– Mix and Match in Channel Sim: Use build in ADS TX with an AMI RX and vice-versa.<br>– NRZ and PAM4 signal to Channel Simulation.<br>Lab: - Add the CILD and the Via models to the Channel and optimize. Use BatchSim to vary both width and spacing of the coupled lines. Use IBIS-AMI components to do bit-by-bit or statistical Channel Simulations. Do eye measurements including density, bathtub and BER on the previously created EM models.<br>*Add EESOF PAM-4 IBIS-AMI Models to Channels Simulation<br>*** if requested** |
| ☐ **Day 3**<br><br>**One day Post-Layout**<br><br>**9AM – 5PM** | **SIPro**<br>– BRD/ODB Import<br>– setup SI simulations in SIPro<br>– Create power-aware SI Analysis, Perform power-aware SI Analysis and S-Parameters and TDT/TDR results.<br>– Learn how to plot single ended and mixed mode s-parameters<br>– Create and use Eye diagrams to investigate Signal Lines behavior in the presence of noise in Power Plane, Understand the role of Power-Aware in SI simulations<br>– Lab: Setup an SiPro Analysis<br>– Lab: Create and use Eye diagrams to investigate Signal Lines behavior in the presence of noise in Power Plane, Understand the role of Power-Aware in SI simulations<br>**PIPro** + **DC IR Drop Electro Thermal**<br>– Learn how to create a PI simulation in SIPro.<br>– Learn about PI-AC analysis, PDN Impedance, S-Parameters, 3D Fields, current density plots.<br>– Learn about Static IR Drop Analysis. Define PI-DC analysis: run and view analysis, interpret the results: Sinks, Pins, VRMs, vias, View Voltage, Current Density, and Power Loss Density plots.<br>– Learn about PDN Impedance Analysis<br>– Electro-Thermal Analysis: Electro-Thermal simulator for DC conditions on a PCB. Perform PI-DC IR-Drop Analysis. And perform PI-DC IR Drop Electro Thermal analysis on imported board.<br>– Lab: Define PI-DC analysis: run and view analysis, interpret the results: Sinks, Pins, VRMs, vias, View Voltage, Current Density and Power Loss Density plots<br>– Lab: Perform PI-DC IR-Drop Analysis on PandaBoard<br>Perform PI-DC IR Drop Electro Thermal analysis on PandaBoard |

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